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QI PC Enable License

| Part # | Product | Description License pri | ice, EUR |
|---------|--|--|----------|
| QIR1100 | QI PC enable license (workstation/node-fixed) | QI enable license is required for every PC/test station that runs Quick Instruments. This option is bound to a particular PC hardware and has to retire together with the PC. PC transfer options are also available on request (within 5-year period from date of purchase) in case of PC failure or premature scrapping. | 2450 |
| QIR1101 | QI PC enable license (dongle-based, flexible) | QI enable license is required for every PC/test station that runs Quick Instruments. This option allows full flexibility, as it allows the same single license to be run from any arbitrary PC at a time. The license is bound to a dongle. | 4250 |
| QIR9100 | PC enable license transfer fee | When QIR1100 has to be transferred from one PC to another, a one-time transfer fee has to be implemented | 350 |

OI FPGA Instruments

Prices per FPGA part name*

| D1- // | I I | QI FPGA Instruments Prices per FPGA I | _ |
|---------|---|---|-----------|
| Part # | Instrument Type | Description License p | rice, EUR |
| QIS1200 | Frequency Counter | Universal non-invasive pulse/oscillator frequency counter on arbitrary FPGA inputs, including differential and reference clock pins (incl. those of MGT transceivers and RF ADC/DAC clocks). | 490 |
| QIS6100 | Fast Flash IC Programmer | Fast link from JTAG to serial (SPI) Flash through the FPGA logic. The instrument receives image, programs and verifies the device. Other supported operations are read back, blank check, chip/manufacturer ID check, sector/chip erase. | 1890 |
| QIS1500 | Digital Pattern Generator | Generates arbitrary digital pattern of a given length on FPGA's any digital output pin. | 1190 |
| QIS3100 | Ethernet Basic Tester | Tests communication over Ethernet link performing structural tests, incl. send/receive ARP/PING packets. Supports GMII/RGMII/RMII/MII interfaces and 1000/100/10Mbps link speed, external/internal loopback test, PHY-to-PHY test or PHY-to-PC test. License includes up to 2 part names* | 950 |
| QIS3108 | Ethernet Stress Tester | Evaluates link quality by measuring Frame Error Rate (FER) during functional test. Supports external/internal loopback and PHY-to-PHY tests, SGMII/GMII/RGMII/MII interfaces and 1000/100/10Mbps link speed. License includes up to 2 part names* | 1190 |
| QIS3500 | Video Interface Tester | Instrument for TMDS/HDMI video link that works as transmitter/receiver or both. It sends adjustable video patterns via video PHYs and counts mismatched pixels. Supports major display standards FullHD, XGA, VGA & colors (RGB, YUV). | 1890 |
| QIS2300 | UART Tester | Sends and/or receives data over UART links, intended to test UART/RS232/RS485/RS422/etc interfaces. License includes up to 2 part names* | 490 |
| QIS2101 | High-Speed I2C / SMBus Tester | High-performance instrument for sending/receiving data over I2C and SMBus interfaces. Allows rapid configuration and programming of popular on-board peripheral devices (clock signal generators, EEPROMs, power controllers, temperature/voltage sensors). Instrument includes QIS2100 license. | 890 |
| QIS5100 | Memory Interconnect Tester | At-speed test solution for interconnection lines between the host FPGA and a DDR memory device. All DDR types are supported DDR4/DDR3/DDR2. | 1090 |
| QIS5102 | DDR Margining Tester (Xilinx 7 Series) | An additive option, which evaluates data signals quality by building BER diagrams. Tests for delays and other timing related faults. Screens out marginal defects, e.g. minor delays, crosstalk, missing ground, etc. NB! Requires QIS5100 Memory Interconnect Tester | 2990 |
| QIS7100 | RF Channel Tester | Test solution for RF links attached to integrated data converters (high-speed ADC/DACs). Sends a continuous software-defined signal and/or converts acquired signal into a set of sampling points. Various test setups are supported (external loopback, test with external equipment like spectrum analyzer and/or signal generator). | 8990 |
| QIS8100 | BER Tester (BERT) | Bit-Error Rate Test/Measurement (BERT) instrument generates/receives PRPG sequences on arbitrary high-speed serial links (FPGA gigabit transceiver). Both loopback and FPGA-to-FPGA configurations supported. Combination of families/vendors is supported. Suitable for testing SMA, SFP/QSFP, Ethernet 10G/40G links and others. Some buses may require dedicated protocols. License includes up to 2 part names* | 2690 |
| QIS8108 | Eye BERT with Mask | An additive graphical option for series/mass production test enabling quick and fully automated quality check based on Statistical Eye Diagrams. Helps to reveal hidden/marginal defects and other assembly quality issues. NB! Requires QIS8100 BER Tester License includes up to 2 part names* | 1790 |

| QIS8201 | PCI Express BERT | An additive option for BERT - adds PCI Express bus protocol handling for establishing communication and loopback options. Requires at-least the basic BERT. NB! Requires QIS8100 BER Tester Lead time: project-dependent | ASK |
|---------|--|---|------|
| QIS8203 | SDI BERT | Adds SDI protocol handling for establishing communication and loopback options. NB! Requires QIS8100 BER Tester Lead time: project-dependent | ASK |
| QIS8204 | JESD204 BERT | Adds JESD204 protocol handling for establishing communication and loopback options. NB! Requires QIS8100 BER Tester Lead time: 6 weeks | ASK |
| QIS1400 | IEEE 1149.8.1 and IEEE 1149.6 instruction support IP | SELECTIVE_TOGGLE, EXTEST_TRAIN and EXTEST_PULSE emulation on an arbitrary FPGA I/O pin. Lead time: 3 weeks | 1190 |

^{*} License for some instruments includes up to 2 part names

QI Software Instruments

Prices per IC part name*

| Part # | Instrument Type | Description License pri | ce, EUR |
|---------|--------------------------|---|---------|
| QIS1100 | PinTouch | A versatile tool to test on-board LEDs, switches, push buttons, jumpers, simple devices and pin-to-pin connections to/from FPGA. Drive, sense, toggle arbitrary pins on FPGA in a static manner. License includes up to 2 part names* | 1590 |
| QIS1300 | ADC Measurement (Xilinx) | Instrument fetches measurements from FPGA's built-in analog-to-digital converters allowing to measure supply voltages and values on external analog pins as well as FPGA core's temperature. | 590 |
| QIS2100 | I2C Tester | I2C / IIC bus integrity test and communicationd solution. Instrument automatically scans I2C bus, enumerates all connected slave devices, sends and receives data (single/multiple bytes) to/from I2C / IIC devices (e.g. on-board sensors, power manager devices, etc). | 490 |
| QIS2200 | SPI Tester | Easy-to-use configurable instrument for SPI bus integrity test and communication. Writes and reads bytes via SPI protocol in different communication modes (CPOL / CPHA). | 490 |
| QIS5101 | DDR4 Connectivity Tester | Test and diagnostics solution for the electrical continuity of pin interconnections between DDR4 memory and the host device (memory controller) on FPGA. Test covers data/address busses as well as memory control signals and follows the JEDEC standard for DDR4 memories (Connectivity Test Mode). | 590 |
| QIS6200 | SVF Player | A solution to program CPLDs via SVF files, control Boundary Scan devices and perform other arbitrary user-defined actions on JTAG bus. | 350 |

^{*} License for some instruments includes up to 2 part names IC support checking on request

FPGA IPs & Stand-Alone Instruments

Prices per FPGA part name

| Part # | Instrument Type | Description License p | rice, EUR |
|---------|--------------------------------|--|-----------|
| QIP6100 | Short configurable BS register | Short reconfigurable Boundary Scan register for speeding-up BS shift operations for different purposes, like e.g. flash programming. Compatibility with EXTEST and other BScan commands as well as with third-party JTAG software tools is ensured via BSDL file modification (included). Lead time: 2 days | 1890 |
| QIP1900 | IO conditioning IP | Setting electrical parameters (terminations, I/O standard, etc) on arbitrary pins for correct signal conditioning, e.g. for IEEE 1149.6 support. Lead time: 2 days | 590 |
| QIP9100 | JTAG to system bus bridge IP | Bridge IP to access embedded system bus of FPGA (AXI/Avalon/PLB) from JTAG port. Provides interoperability between FPGA's functional firmware and external JTAG test controller. Capable to execute read/write cycles on system bus, i.e. to comminucate with FPGA's peripheral cores. Requires intergation into 3rd-party functional / mission-mode firmware. Lead time: 2 weeks | 3290 |

Customization and deployment service

| Part # | Service | Price, EUR/h |
|---------|---|--------------|
| QID9900 | Custom embedded FPGA/SW instrument development | 129 |
| QID9901 | Embedded SW deployment service. Integration into customer's test runtime (LabVIEW, TestStand, etc.) | 129 |
| QID9909 | Customization for engineering changes | 129 |

Standard Conditions

Delivery term: EXW Tallinn, ESTONIA. Prices without VAT.

Standard lead time is 1 day. It is effective for supported FPGA devices in the instrument library.

Warranty: 1 year bug fixes in runtime and instruments

Updates: instruments and runtime can be updated within 1 year from the date of delivery